IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Art Unit	:	
Examiner	:	
Serial No.	:	**Customer No. 26794**
Filed	: Herewith	
Inventors	: Christopher N. Brindle	
Title	: SERIES/SHUNT SWITCH	Docket No.: 17987
	: AND METHOD OF CONTROL	
		Dated: August 26, 2003

PETITION TO MAKE SPECIAL
UNDER 37 C.F. R. § 1.102(d)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicant hereby petitions under 37 C.F.R. §1.102(d) and MPEP 708.02(VIII) that the subject application be accorded special status and advanced in order of examination.

The requirements of 37 C.F.R. §1.102(d) and MPEP 708.02(VIII) are fulfilled as follows:

1. A check for the appropriate fee ($130.00) as set forth in 37 C.F.R. §1.17(h) is attached hereto.

2. The patent application as filed presents Claims 1-23 drawn to a single invention. In the event restriction is required, an election will be made without traverse.

3. A pre-examination search was made. The classes and subclasses searched were 327/428, 430, 436, 404, 104, 309, 428, 581; 361/56, 91.5, 111. An Information Disclosure Statement (IDS) is filed concurrently herewith. The listed publications, copies enclosed, represent the results of the search.

4. A copy of the cited publications is enclosed for the record.

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5. A detailed discussion of the publications follows, pointing out, with particularity as set forth in 37 C.F.R. §§ 1.111(b) and (c), that the claimed subject matter is patentable over the cited publications.

Applicants respectfully submit that all requirements called for by the applicable rules have been fulfilled. Applicants respectfully request early favorable action on this Petition.

DETAILED DESCRIPTION OF THE CITED ART

This detailed description of the related art is submitted as part of the Petition to Make Special pursuant to 37 C.F.R. §1.102(d) and MPEP 708.02. The following publications were uncovered during the pre-examination search and are discussed below:

No.	Patent No.	Inventor	Date Issued	Title
U.S. Patents				
1.	3,731,116	Hill	05/01/1973	High Frequency Field Effect Transistor Switch
2.	4,158,149	Otofuji	06/12/1979	Electronic Switching Circuit Using Junction Type Field-Effect Transistor
3.	4,678,929	Alpaiwalla et al.	07/07/1987	Radio Frequency Switch
4.	4,742,249	Alpaiwalla et al.	05/03/1988	RF Switch with Diode Network and Control Latch Sharing Common Element
5.	5,107,152	Jain et al.	04/21/1992	Control Component for a Three-Electrode Device
6.	5,301,081	Podell et al.	04/05/1994	Input Protection Circuit
7.	5,705,940	Newman et al.	01/06/1998	Logic Family for Digitally Controlled Analog Monolithic Microwave Integrated Circuits
8.	5,717,356	Kohama	02/10/1998	Low Insertion Loss Switch
9.	5,818,099	Burghartz et al.	10/06/1998	MOS High Frequency Switch Circuit Using a Variable Well Bias
10.	5,818,283	Tonami et al.	10/06/1998	High Power FET Switch
11.	US2001/0023 3206A1	Constantine et al	10/25/2001	Phase Compensated Switched Attenuation Pad

1. **U.S. Patent No. 3,731,116 to Hill**

This patent discloses an improved field effect transistor (FET) switching circuit for sampling an analog input in response to a control pulse at extremely fast turn-on and turn-off times, the FET operating potential is obtained from a constant voltage source rather than the control signal. A diode is provided between the FET gate and the signal source and also a diode is provided between the FET gate and the control pulse source; the diodes retain sufficient stored charge to completely discharge the FET gate to channel capacitance during switching.

2. **U.S. Patent No. 4,158,149 to Otofuji**

This patent discloses an electronic switching circuit using a junction type field-effect transistor, a capacitor is connected between the gate electrode of the transistor and a control pulse source. The capacitor is cooperative with a rectifying action of the gate electrode of the transistor to supply to the gate of the transistor a switching voltage which is different from the potential level of the control pulse from the control pulse source and is DC-restored following an input signal applied to the transistor.

3. **U.S. Patent No. 4,678,929 to Alpaiwalla et al.**

This patent discloses a radiofrequency switch, in which a pair of diodes is coupled in series with polarities opposed between input and output ports. A shunt diode is coupled between the junction point of the pair of diodes and a point of reference potential. When the switch is to couple a signal between the input and output ports, a control arrangement applies bias tending to forward bias the pair of diodes, to reverse bias the shut diode and cut off conduction through the transistor. When the switch is not to couple a signal, the control arrangement applies bias tending to reverse bias the pair of diodes, forward bias the shunt diode, and to bias the transistor into a highly conductive condition, thereby further reducing any difference of potential between

the junction point and the point of AC reference potential and cooperating with the bias potential tending to forward bias the shut diode and reverse bias the pair of diodes. In another embodiment, one diode of the pair of diodes is coupled to the junction point by way of a low-pass filter which does not substantially affect a signal to be coupled but exhibits a high series impedance which increases the attenuation when the switch is not to couple a signal.

4. U.S. Patent No. 4,742,249 to Alpaiwalla et al.

This patent discloses a diode network including a series branch coupled between two signal ports and a shunt branch coupled between a node in the series branch and ground and connected in parallel with a transistor of a latching circuit that is further coupled to supply forward bias to the shunt branch and reverse bias to the series branch when the transistor is conductive for blocking RF signal flow between the ports. The bias applied to the branches is reversed when the latch transistor is non-conductive thereby enabling RF signal flow between the ports. The transistor provides plural functions of establishing positive feedback for the latch, supplying forward and reverse bias to the shunt and series branches, respectively, and enhancing the attenuation of the shunt branch when conductive.

5. U.S. Patent No. 5,107,152 to Jain et al.

This patent discloses a gate biasing circuit including a Schottky barrier diode in series with an ion implanted resistor for use with a baseband MMIC control components such as an MESFET. The diode gate biasing scheme improves the low frequency distortion characteristics of GaAs MESFET control components significantly, allowing microwave power handling and distortion characteristics to be maintained below 100 Hz.

6. **U.S. Patent No. 5,301,081 to Podell et al.**

This patent discloses a depletion-mode MESFET is connected between an RF input terminal and ground. The gate is connected to a negative reference voltage via a bias resistor and to ground via a capacitor. A detector couples the input terminal to the gate and includes first and second series diodes and a second resistor connected from between the first and second diodes to ground. A coil is connected between the input terminal and an output terminal connected to a GaAs integrated circuit. A Schottky diode limiter is connected to the output terminal for limiting the voltage of both positive and negative polarities that leak to the output terminal from the transistor.

7. **U.S. Patent No. 5,705,940 to Newman et al.**

This patent discloses a transmit/receive module including digitally controlled analog circuits. The digital circuits use a logic family adapted for use with analog monolithic integrated circuits. The disclosure also describes a preferred process to provide digital and analog microwave circuits on a common semiconductor substrate.

8. **U.S. Patent No. 5,717,356 to Kohama**

This patent discloses a switching circuit further decreasing the insertion loss. The first capacitor is connected between the drain terminal of the field effect transistor and the ground and/or the second capacitor is connected between the source terminal of the field effect transistor and the ground, and the capacitances of the first and/or second capacitances are set to optimum values. Accordingly, the switching circuit can be easily obtained which is low in insertion loss at a desired frequency. Besides, since a bias circuit for generating bias voltage from control voltage which is applied to the two control terminals of a switching circuit using a field effect

transistor is provided, a switching circuit which does not need exclusive bias terminals and is superior in isolation property can be realized.

9. U.S. Patent No. 5,818,099 to Burghartz

This patent discloses an RF switch comprising a switching FET having gate and back gate terminals, an input port for receiving an RF signal, and an output port for providing substantially the RF signal during the ON state of the FET. Switching circuitry connects the back gate terminal of the FET to the input port during the ON state to reduce insertion loss during the ON state, and connects the back gate terminal to a point of reference potential during an OFF state of the FET to increase isolation during the OFF state. Preferably, the switching FET is a depletion mode silicon MOSFET capable of operating with low supply voltages. The switching circuitry preferably comprises a second FET for electrically connecting the back gate terminal and the input terminal (e.g., source) of the switching FET during the ON state, and a third FET for electrically connecting the back gate terminal of the switching FET to the point of reference potential during the OFF state.

10. U.S. Patent No. 5,818,283 to Tonami et al.

This patent discloses a FET switch for controllably allowing and inhibiting passage of an input signal in ON state and OFF state, respectively, in which FETs are connected in a multi-stage configuration. A control voltage adjusting circuit is connected between a gate and one of a drain and a source of each FET. The control voltage adjusting circuit adjusts a gate-source voltage so as to follow the variation of a drain-source voltage. The input voltage applied to the FET switch in OFF state is divided by the plurality of FETs. Since the variation of the gate-source voltage follows the variation of the drain-source voltage, the FET switch is hardly influenced by an amplitude of the input signal.

11. U.S. Patent Application Publication No. US2001/0033206A1 to Constantine et al.

This patent application discloses a phase compensated switched attenuation device **6** for attenuating high frequency signals while maintaining an insertion loss of less than 1 dB up to 3 GHz. A single GaAs FET **12** is coupled between input port **8** and output port **9** in parallel with a 20 dB pad **10** for switching the device **6** between a through state and an attenuation state. First and second isolation FET's **14** and **16** are coupled between the GaAs FET **12** and pad terminals **18** and **19** to isolate the GaAs FET **12** is on, and increase isolation of the GaAs FET **12** from the pad **10** when the GaAs FET 12 is on. A resistor **24** or a series combination of a resistor **24** and capacitor **26** can be coupled to the pad terminals **18** and **19** in parallel with the pad **10** to improve return loss when the GaAs FET **12** is on. Resistors **21, 22,** and **23** are also provided to reduce distortion, coupling gates of the FET's **12, 14** and **16** to a plurality of voltage references V1 and V2.

DESCRIPTION OF THE INVENTION

The present invention relates in general to switch devices, and more particularly to a series/shunt FET switch between two signal ports.

ANALYSIS OF THE CITED ART

Claims 1, 2, 3, 6, 8 and 9 are representative of aspects of the invention. These claims are reproduced below for the Examiner's convenience.

> **"1. An integrated circuit switch comprising:**
> **at least two signal ports coupled by a signal path, the signal path including a channel of at least one series FET;**
> **a shunt path coupled to ground and including a channel of a shunt FET; and**

a control voltage applied to a gate of the series FET and to a drain/source of the shunt FET."

"2. A method for switching a signal so as to selectively connect a first port to an integrated circuit, comprising:

providing a series switch in a signal path between the first port and the second port;

providing a shunt switch in a shunt path coupled to ground; and

using a common logic signal to control both the series switch and the shunt switch."

"3. A switch for coupling a first port to a second port, comprising:
a control signal input;

at least one series FET connected tin series between the first port and the second port, said at least one series FET having a gate coupled to the control signal input; and a shunt path including a shutn FET, the shunt FET having a drain and source coupled to the control signal input and to the gate of said at least one series FET, whereby a single control signal is applied to both said at least one series FET and the shut FET, via the control signal input, in order to turn said at least one series FET on and simultaneously turn the shunt FET off and, conversely, in order to turn the series FET off and simultaneously turn the shunt FET on."

"6. A switch for coupling a first port to a second port, comprising:

a control signal input;

an FET connected in series between the first port and the second port, said series FET having a gate coupled to the control signal input; and

means for enhancing the isolation between the first and second ports, and for improving the harmonic noise rejection of the switch, the isolation and harmonic rejection means having an input coupled to the control signal input and to the gate of the series FET, whereby a single control signal is applied to both the series FET and the isolation and harmonic rejection means, via the control signal input, in order to turn the series FET on and simultaneously turn the isolation means off and, conversely, in order to turn the series FET off and simultaneoulsy turn the isolation means on."

"8. A method of controlling the coupling of a first port to a second port via a series/shunt FET switch, comprising the steps of:

isolating the first port from the second port, using a single control signal, by turning off a series FET by biasing the gate-source voltage of the series FET below the pinchoff voltage; and

coupling the first port to the second port, using a single control signal, by turning on the series FET by biasing the gate-source voltage above the pinchoff voltage, and turning the shut FET off by biasing the gate-source voltage above the pinchoff voltage."

"9. An integrated circuit for selectively connecting and disconnecting a first RF port to or from a second RF port, comprising:

a signal path connecting the first RF port and the second RF port;

at least one switching transistor having a signal path and a control electrode, a first control voltage applied to the control electrode rendering the current path to be of high impedance; and

a shunt transistor having a diverging signal path, one end of the signal path of the shunt transistor coupled to the control electrode (gate) of said at least one series switching transistor, a second end of the signal path of the shunt transistor coupled through a low signal impedance to the signal ground reference; additionally allowing for control of the shunt transistor signal path impedance by application of the first control voltage to both the control electrode (gate) of the series transistor and simultaneously to the drain and/or source of the shunt transistor rendering the signal path of the shunt transistor substantially nonconductive while the series transistor signal path is conductive, and wherein application of the second control voltage to the shunt transistor renders the signal path of the shunt transistor conductive while the series transistor path is simultaneously nonconductive with the same second control voltage simultaneously applied to its control electrode (gate) to thereby increase the isolation between the first and second ports."

U.S. Patent No. 3,731,116 to Hill discloses an improved field effect transistor (FET) switching circuit for sampling an analog input in response to a control pulse at extremely fast turn-on and turn-off times, the FET operating potential is obtained from a constant voltage source rather than the control signal. The Hill patent nowhere teaches or suggests the claimed switch comprising at least two signal ports in series with at least one series FET connected therebetween, and a shunt path having a FET, whereby a control voltage is applied to a gate on the series FET and to a drain on the shunt FET.

U.S. Patent No. 4,158,149 to Otofuji discloses an electronic switching circuit using a junction type field-effect transistor, a capacitor which is connected between the gate electorde of the transistor and a control pulse source. The Otofuji patent nowhere teaches or suggests the claimed switch comprising at least two signal ports in series with at least one series FET connected therebetween, and a shunt path having a FET, whereby a control voltage is applied to a gate on the series FET and to a drain on the shunt FET.

U.S. Patent No. 4,678,929 to Alpaiwalla et al. discloses a radiofrequency switch, a pair of diodes coupled in a series with polarities opposed between input and output ports. The Alpaiwalla patent nowhere teaches or suggests the claimed switch comprising at least two signal ports in series with at least one series FET connected therebetween, and a shunt path having a FET, whereby a control voltage is applied to a gate on the series FET and to a drain on the shunt FET.

U.S. Patent No. 4,742,249 to Alpaiwalla et al. discloses a diode network including a series branch coupled between two signal ports and a shunt branch coupled between a node in the series branch and ground and connected in parallel with a transistor of a latching circuit that is further coupled to supply forward bias to the shunt branch and reverse bias to the series branch when the transistor is conductive for blocking RF signal flow between the ports. The Alpaiwalla patent nowhere teaches or suggests the claimed switch comprising at least two signal ports in series with at least one series FET connected therebetween, and a shunt path having a FET, whereby a control voltage is applied to a gate on the series FET and to a drain on the shunt FET.

U.S. Patent No. 5,107,152 to Jain et al. discloses a gate biasing circuit including a Schottky barrier diode in series with an ion implanted resistor for use with a baseband MMIC control components such as an MESFET. The Jain patent nowhere teaches or suggests the claimed switch comprising at least two signal ports in series with at least one series FET connected therebetween, and a shunt path having a FET, whereby a control voltage is applied to a gate on the series FET and to a drain on the shunt FET.

U.S. Patent No. 5,301,081 to Podell et al. discloses a depletion-mode MESFET connected between an RF input terminal and ground. The Podell patent nowhere teaches or suggests the claimed switch comprising at least two signal ports in series with at least one series FET

connected therebetween, and a shunt path having a FET, whereby a control voltage is applied to a gate on the series FET and to a drain on the shunt FET.

U.S. Patent No. 5,705,940 to Newman et al. discloses a transmit/receive module including digitally controlled analog circuits. The Newman patent nowhere teaches or suggests the claimed switch comprising at least two signal ports in series with at least one series FET connected therebetween, and a shunt path having a FET, whereby a control voltage is applied to a gate on the series FET and to a drain on the shunt FET.

U.S. Patent No. 5,717,356 to Kohama discloses a switching circuit further decreasing the insertion loss. The Kohama patent nowhere teaches or suggests the claimed switch comprising at least two signal ports in series with at least one series FET connected therebetween, and a shunt path having a FET, whereby a control voltage is applied to a gate on the series FET and to a drain on the shunt FET.

U.S. Patent No. 5,818,099 to Burghartz et al. discloses a RF switch comprising a switching FET having gate and back gate terminals, an input port for receiving an RF signal, and an output port for providing substantially the RF signal during the ON state of the FET. The Burghartz patent nowhere teaches or suggests the claimed switch comprising at least two signal ports in series with at least one series FET connected therebetween, and a shunt path having a FET, whereby a control voltage is applied to a gate on the series FET and to a drain on the shunt FET.

U.S. Patent No. 5,818,283 to Tonami et al. discloses a FET switch for controllably allowing and inhibiting passage of an input signal in ON state and OFF state, respectively, in which FETs are connected in a multi-stage configuration. The Tonami patent nowhere teaches or suggests the claimed switch comprising at least two signal ports in series with at least one

series FET connected therebetween, and a shunt path having a FET, whereby a control voltage is applied to a gate on the series FET and to a drain on the shunt FET.

U.S. Patent Application Publication No. US2001/0033206A1 to Constantine et al. discloses a phase compensated switched attenuation device **6** for attenuating high frequency signals while maintaining an insertion loss of less than 1 dB up to 3 GHz. The Constantine application nowhere teaches or suggests the claimed switch comprising at least two signal ports in series with at least one series FET connected therebetween, and a shunt path having a FET, whereby a control voltage is applied to a gate on the series FET and to a drain on the shunt FET.

Accordingly, Applicants respectfully request that the Petition to Make Special be granted, and that the application be taken out of turn for examination. Applicants also respectfully request an early consideration and allowance of the solicited claims.

Respectfully submitted,

Paul A. Taufer
Reg. No. 35,703

PAT:ers
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